SESSION 8 – TAPA I
Flash Memory I

Wednesday, June 16, 8:00 a.m.
Chairpersons: D. Shum, Infineon
S. Onishi, Sharp

8.1 — 8:00 a.m.

Vertical Floating-Gate 4.5F² Split-Gate NOR Flash Memory at 110nm Node, D. Lee, F. Tsui, J.-W. Yang, F. Gao, W.-J. Lu, Y. Lee, C.-T. Chen, V. Huang*, P.-Y. Wang*, M.H. Liu* H.C. Hsu*, S. Chang*, S.Y. Chang, H.V. Tran, J. Frayer, Y.-W. Hu, B. Yeh and B. Chen, Silicon Storage Tech., Inc., Sunnyvale, CA, *PowerChip Semiconductor Corp., Hsin-Chu, Taiwan, ROC

We present the structural and electrical characteristics of the latest generation of a self-aligned split-gate NOR memory incorporating a vertical floating-gate channel having 4.5 feature squared area on 110nm half-pitch rules. With enhanced electric fields for erase and programming, the cell achieves erase time <1ms and program time < 10 microseconds at 100nA programming current. These results demonstrate continued scalability of the Super Flash cell for high-density, high-speed applications.

8.2 — 8:25 a.m.

Scanrom, a Novel Non-Volatile Memory Cell storing 9 Bits, M. Rosmeulen, J. Van Houdt, L. Haspeslagh and K. De Meyer, IMEC, Leuven, Belgium

We present a novel non-volatile memory cell based on a dual-gate transistor with an ONO charge-trapping dielectric underneath the drain-side gate. Multiple bits are stored along the width of the device. By contacting the gates from both sides and applying an appropriate bias difference to each, the individual bits are addressed for both reading and writing. We experimentally demonstrate reading and writing of 9 bits in a prototype cell.

8.3 — 8:50 a.m.

110nm NROM Technology for Code and Data Flash Products, J. Willer, C. Ludwig, J. Deppe, C. Kleint, S. Riedel, J.-U. Sachse, M. Krause, R. Mikalo, E. v. Kamienski, S. Parascandola, T. Mikolajick, J.-M. Fischer, M.Isler, K.-H. Kuesters, I. Bloom*, A. Shapir*, E. Lusky* and B. Eitan*, Infineon Tech. Flash, Dresden, Germany, *Saifun Semiconductors, Netanya, Israel

A novel NROM generation with a bit size of 0,043µm²/bit at a 110nm design rule is introduced. The concept features mainstream CMOS type cell devices in conjunction with a metal contact based virtual ground array architecture. The new technology node serves both advanced code flash products and file storage memories up to 2 Gbit/die.

8.4 — 9:15 a.m.

Split-Gate NAND Flash Memory at 120nm Technology Node Featuring Fast Programming and Erase, C.-Y. Hsu, C.-W. Hung, D. Sung, C.-S. Wu, S.C. Chen, H.H. Kuo, J.Y. Pan, C.L. Chen, I.C. Chuang, V. Huang, C.C. Hsue, D.-T. Fan*, J.-C. Lu*, C.Y.-S. Cho*, K. Tseng*, A. Hsu**, B. Sheen**, P. Tuntasood** and C.-F. Chen*, PowerChip Semiconductor Corporation, Hsin-Chu, Taiwan, ROC, *Actrans System, Inc., Hsin-Chu, Taiwan, ROC, **Actrans Systems, Inc., Santa Clara, CA

For the first time, split-gate NAND flash memory featuring inter-poly erase and mid-channel programming is demonstrated at 120nm technology node. The cell array operates at single polarity voltages lower than 12V. Erase and programming can be accomplished in 0.5ms and 10us, respectively.

8.5 — 9:40 a.m.

A Novel MNOS Technology Using Gate Hole Injection in Erase Operation for Embedded Nonvolatile Memory Applications, F. Ito, Y. Kawashima, T. Sakai, Y. Kanamaru, Y. Ishii, M. Mizuno, T. Hashimoto, T. Ishimaru*, T. Mine*, N. Matsuzaki*, H. Kume*, T. Tanaka, Y. Shinagawa, T. Toya, K. Okuyama, K. Kuroda and K. Kubota, Renesas Technology Corporation, Ibaraki, Japan, *Hitachi, Ltd., Tokyo, Japan

A novel MNOS memory with gate hole injection in erase operation has been demonstrated for embedded nonvolatile memory applications. Superior characteristics with 10usec programming and 10msec erasing speed were obtained as compared with conventional MONOS structures. In addition, we found that the localized interface trap at source side region was generated by excess holes during erasing cycle and could be suppressed by Lg scaling. This result shows the good scalability of this technology.